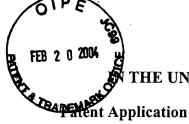


W/// Date: February 18, 2004

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for

Patents, P.O. Box 1450, Alexandria, VA 22313-1450



THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Luk et al.

Docket No.:

YOR920030604US1

Serial No.:

10/751,713

Filed:

January 5, 2004

Group:

Unassigned

Examiner:

Unassigned

Title:

i.

3T1D Memory Cells Using Gated Diodes and Methods of Use Thereof

Signature

TRANSMITTAL OF FORMAL DRAWINGS

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Attention: Official Draftsperson

Sir:

Applicants submit herewith twenty-three (23) sheets of formal drawings and an Associate Power of Attorney in the above-referenced application.

Respectfully submitted,

Date: February 18, 2004

Robert J. Mauri Attorney for Applicants

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